User Module Bus troubleshooting

Introduction
This note describes possible problems that can cause a “Bus Error” alarm on a UMB\(^1\). The proposed systematic approach will help you to analyze and cure the problem. The UMB originates from a “Structured RTC SO Interface module” (SPS10198), which distributes the user register data over the bus. For the sake of simplicity I will from now on refer to the “Structured RTC SO Interface module” as UMB Master. The UMB Master communicates with the ECA across 2 LEMO 00 (Triggers) and 1 SMC connector (Serial Link) see section on UMB Master Connections. Connector names are written in Arial font to improve the readability.

Bus Error
The UMB Master distinguishes 3 possible error conditions indicated by LEDs on it’s frontpanel:
- Comm. Time-out
- Bad Parity
- Module No Ack.

The 1\(^{st}\) and 2\(^{nd}\) error are both fatal and will cause the UMB Master sequencer to be forced back to it’s Idle state. Like this, any possibly corrupted data will never be brought online. All online equipment registers will maintain their values. The 3\(^{rd}\) error is non fatal and the UMB continues to function as far as possible. The UMB Master has a summary alarm output, which connects to either BCALRM (BA3) or BTDmp1 (BA2) for the alarm transmission. On the Alarm console such an alarm shows like:

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RF_SPS_DAMPER USER_MODULE_BUS_V_A Bus Error
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The sections below describe the 3 distinguished errors in detail.
- Before actually going to inspect the equipment always reload, or ask the PCR operator to reload, the UMB from the MMI “actif” to ensure the RTC contents to be correct. If the alarm persists you’ll have to go to the UMB Master and watch it’s error LEDs.
- Arrived near the UMB Master verify if it receives the STOP/START trigger for each cycle start. If this trigger is missing you should:
  - First verify if the ECA’s cycle trigger receiver (SPS 10236) is receiving the cycle triggers -> Green flash LED.
    - If yes, verify the Lemo 00 link from the Cycle trigger receiver’s Cycle Trigger output to the UMB Master’s Start input.
    - Otherwise check the Cycle Data SD in (SMC) coming from the Cycle timing crate. Note that this Cycle timing signal can also be routed via an adjacent ECA see: [http://cern.ch/SPS-RF-Piquet/Controls/ECA/distr_fc.pdf](http://cern.ch/SPS-RF-Piquet/Controls/ECA/distr_fc.pdf)

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\(^1\) UMB = User Module Bus.
• For a correct functioning, the UMB Master should also receive a Next trigger in certain or all cycles. Without this Next trigger data will be distributed every cycle but this data will never come online.
• The UMB Master display should also show correct values concerning Cycle, Parameter set and Register count. The LEDs Reg 0 and Reg 1 show which side of the display (left or right) corresponds to the Online “register set”. Upon a cycle change the Offline Cycle should show a (hex) number corresponding to the RTC stack, while the Parameter set must be “01”. The Register count display should always show the same (hex) value in both On and Offline sides and corresponds to the number of implemented (16 bit) registers declared on the UMB (MMI database).
• Now observe which error you get and during which cycle. If this cycle is not supposed to execute you could try reloading the Cycle timing crate (BA3 crate 00, BA2 crate 20). If the error is independent of the cycle, proceed to the error related checks, see below.

Comm. Time-out
The communication link between the UMB Master and the ECA is malfunctioning. Either the RTC Serial data or the UMB Master RTC trigger is disconnected.
• Check if the RTC-SO “active” LED flashes at least once per cycle.
  o If YES, the problem concerns the RTC Serial data not arriving at the UMB Master. Check the Serial Link cabling (isolated SMC SD in on UMB Master).
  o If NO, the RTC triggers coming from the UMB Master do not arrive at the RTC. Check the RTC trig. Cable (LEMO 00).

Bad Parity
The parameter set header and register data parity is not correct. This error can occur due to:
1. RTC uninitialized data,
2. An internal problem in the ECA (RTC, cabling or RTC Serial out),
3. A problem with the cable (very unlikely).
The ECA’s RTSo write conversion routine automatically calculates the overall parity and writes it (as part of the parameter set) to the RTC memory.

Module No Ack.
If for whatever reason any of the user registers declared on the UMB, from 1 to Register count, do not acknowledge their address by pulling the UMB Acknowledge (not) line with its open collector output, this error occurs. Possible causes are:
• An address selector of a user module / UMB distributor (SPS10200) has been moved by accident.
• The UMB flat cable is disconnected, badly inserted or has degraded contacts.
• A user module has lost power.
The offending module can be found by connecting a UMB distributor to the UMB and perform a scan through the used address space (step one of the Register address selectors, one step per cycle, from 1 to Register count). As soon as you have selected the address of the offending module the error will disappear. This address allows you to identify the culprit. If more than one user Module fail to acknowledge this method
will not work and you could measure the UMB Ack. and MSS signal with a DSO\(^2\) see appendix: UMB signals and MSS Diagnostic output.

**Appendix**

**UMB Master connections**

The UMB Master requires the following connections to function:

- SD in \(<-\) RTC SO (ECA RTC Serial out 0/1, 2/3…)
- RTC trig. \(\rightarrow\) RTC user trigger (0/1, 2/3…) See also Note below.
- Start \(<-\) ECA Cycle trigger out (a,b,c,d or buffered)
- Next \(<-\) Timing system or User generated trigger.

Optional are:

- Stop \(<-\) Trigger (Only used in Stop / Start mode; default is StopStart)
- Alarm \(\rightarrow\) A floating contact compatible with the BCALRM crate type of interface.

See also the figure below:

**Note:** In the case of the Damper the RTC Us\_trig of the 2 UMBs sharing the same RTC are coming from one of the two UMB Masters. This implementation is a temporary fix for a synchronization problem in the RTC in case of asynchronous concurrent triggering.

\(^2\) DSO = Digital Storage Oscilloscope.
UMB Module overview

The following modules have been developed to interface to the UMB

- The Structured RTC SO Interface (SPS10198 **UMB Master**).
- User Module Interface (SPS10199, Serial link Rx compatible piggy-back). This interface offers a 16 bit parallel interface with strobe corresponding to one register on the UMB.
- Structured RTC SO distributor (SPS10200). This module decodes 4 UMB registers (front panel address selections) and transmits the online register contents to the remote user equipment via individual Serial link outputs. The remote equipment uses a standard Serial link receiver (SPS10240) to get the data.
- Other implementations embedded in a CPLD or FPGA.

The drawing below gives an overview of the possibilities:
UMB signals

The UMB 10 pin flat cable carries 9 signals and a signal ground:

![Diagram of the 10 wire UMB]

**The 10 wire UMB**

- **A4-A0**: User Module Address (1-31)
- **SD**: Serial Data
- **SDclk**: Serial Data clock
- **RS0**: Register Select 0 (Selects On/Offline Register)
- **Mack**: Module Acknowledge (Open Collector pulled by User Interface when addressed)
- **Gnd**: Ground Reference

**Remarks:**
- The Mack should be received by the UMB master upon the first positive SDclk edge and maintained for the duration of a recognised address (7 in the example).
- Address changes occur far (>1 bit-time) from the first active SDclk edge.
- Data changes occur in between active (rising) SDclk edges ($T_{su}$ and $T_{hold} = 320$ ns).
- A register load is complete when it’s Mack (valid address) disappears.
- The UMB Master loads the User Registers from high to low address, the first frame appearing on the UMB has address 0 and contains the SSO header informing the UMB Master of the Register Count. The successive frames are the user data. The data distribution is ready when the UMB address reaches 0.

![Diagram of UMB Timing]

**UMB Timing**

- **MSbit first**
- **LSbit last**

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- The Mack should be received by the UMB master upon the first positive SDclk edge and maintained for the duration of a recognised address (7 in the example).
- Address changes occur far (>1 bit-time) from the first active SDclk edge.
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**MSS Diagnostic output**

The UMB Master offers a diagnostic output (LEMO 00) on it’s front panel called MSS. This MSS is an analogue representation of the UMB Master Main Sequencer State. Each Sequencer state has it’s own output level, about 250mV/state in 50Ω. Note that these levels correspond to the green LEDs on the front of the UMB Master. This MSS output can be connected to a DSO to allow you to correlate this trace with for instance a measurement of signals on the UMB.

The figure below shows a typical waveform:

![UMB Master MSS Diagnostic output](image)

The Main Sequencer States are coded like:

0) Idle: Waiting for **Start**
1) Get_rc: Get Register Count
2) Chk_rC: Checking Register Count
3) Load_reg: Loading UMB register
4) WaLd: Waiting for Serial Link receiver ready
5) WaNe: Waiting for **Next**, **Stop** or **StopStart** trigger.

A practical trigger level is 125mV negative slope which will start the time-base upon a start of cycle.